Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1.   (Previously Presented) An integrated memory system, comprising at least a non-volatile solid-state memory and an automatic storage error corrector, characterized in that the memory system comprises circuit means, functionally independent, each of them being responsible for the correction of a predetermined storage error of data stored in the memory; at least one of said means generating a signal to ask a correction being external to the memory.

2.   (Previously Presented) A system according to claim 1, characterized in that said memory is connected to a controller by means of an interface bus and said circuit means are incorporated both in the memory and in the controller.

3.   (Previously Presented) A system according to claim 1, characterized in that, in the memory, said means comprise:

circuits for the coding required to correct two errors;

a logic for calculating a syndrome;

a circuit for correcting a single error;

a logic for detecting more than one error.

4.   (Original) A system according to claim 3, characterized in that said means also comprise:

a logic for bringing to the controller:

a one-or-no-error-corrected data ;

the uncorrected error; and

the calculated syndrome.

5.   (Previously Presented) A system according to claim 2, characterized in that said circuit means comprise a circuit for generating a signal activated to request the external correction of an error by said controller.

6.   (Previously Presented) A system according to claim 3, characterized in that said coding circuits are located immediately downstream of the input terminal of said memory and perform a vector product proportional to the number of parity bits and obtained through the synthesis of a corresponding logic function.

7.   (Previously Presented) A system according to claim 6, characterized in that said logic for calculating the syndrome uses a parity calculation circuit of the coding circuits.

8.   (Original) A system according to claim 3, characterized in that said circuit for correcting a single error comprises a block for decoding a single error effective to recognise each of the several syndromes associated to a single error to activate, through a corresponding vector, the correction of the corresponding bit.

9.   (Previously Presented) A system, comprising:
        a first circuit operable to store data in a non-volatile solid-state memory, the data having associated therewith at least one storage error of a plurality of storage-error types, the first circuit operable to correct a first-type error of the plurality of storage-error types; and
        a second circuit coupled to the first circuit, the second circuit operable to correct a second-type error of the plurality of storage-error types.

10.   (Original) The system of claim 9 wherein the second circuit is operable to generate a signal requesting correction of a third-type error of the plurality of storage-error types.

11.   (Original) The system of claim 9 wherein the first circuit is further operable to determine at least one syndrome associated with the at least one storage error.

12.   (Original) The system of claim 9 wherein the first circuit is further operable to detect the second-type error.

13.   (Original) The system of claim 9 wherein the second circuit corrects the second-type error in response to a signal generated by the first circuit.

14.   (Original) The system of claim 9 wherein the first circuit comprises a non-volatile memory.

15.   (Original) The system of claim 9 wherein:
        the first circuit is disposed on a first integrated circuit; and
        the second circuit is disposed on a second integrated circuit.

16.   (Original) The system of claim 9 wherein the first and second circuits are disposed on an integrated circuit.

17.   (Previously Presented) A memory device, comprising:
        a non-volatile solid-state storage portion operable to store data having associated therewith at least one storage error of a plurality of storage-error types;
        a first circuit operable to correct a first-type error of the plurality of storage-error types; and
        a second circuit operable to generate a signal indicating detection of a second-type error of the plurality of storage-error types.

18.   (Original) The device of claim 17, further comprising a third circuit operable to determine at least one syndrome associated with the at least one storage error.

19.   (Previously Presented) A method, comprising:
        storing, in a non-volatile solid-state memory location of a device, data having associated therewith at least one storage error of a plurality of storage-error types; and

correcting, at the memory location, a first-type error of the plurality of storage-error types.

20.   (Original) The method of claim 19, further comprising generating, at the memory location, an interrupt-request signal indicating detection of a second-type error of the plurality of storage-error types.

21.   (Previously Presented) An electronic system, comprising:

a first integrated circuit having a non-volatile solid-state memory operable to store data having associated therewith at least one storage error of a plurality of storage-error types, the memory operable to correct a first-type error of the plurality of storage-error types; and

a second integrated circuit coupled to the first circuit, the second integrated circuit having processor operable to correct a second-type error of the plurality of storage-error types.